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J. M. H.  
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Malinowski *et al.*

) Examiner: Thai, Luan C.  
)

Serial No.: 09/683,027

) Art Unit: 2827  
)

Filed: 11/9/01

For: **DUAL CHIP STACK METHOD FOR ELECTRO-STATIC DISCHARGE  
PROTECTION OF INTEGRATED CIRCUITS**

Commissioner for Patents  
Washington, D.C. 20231

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Response to Restriction Requirement

Sir:

In response to the Restriction Requirement dated April 23, 2002, Applicants hereby provisionally elect Group I, claims 1-33, drawn to a semiconductor device, classified in class 257, subclass 777. This election is made with traverse, and Applicants hereby reserve the right to file a divisional application in connection with unelected claims 34-40 drawn to a method of making a semiconductor device.

With regard to the Restriction Requirement, Applicants respectfully submit that the subject matter of all claims 1-40 is sufficiently related that a thorough search for the subject matter of any one group of claims would encompass a search for the subject matter of the remaining claims. Thus, Applicants respectfully submit that the search and the examination of the entire application could be made without serious burden. See MPEP § 803, in which it is stated that "if the search and examination of the entire application can be made without serious burden, the Examiner must examine it on the merits" (emphasis added). Applicants respectfully submit that this policy should apply in the present application in order to avoid unnecessary delay and expense to Applicants and duplicative examination by the Patent Office.

Should the Examiner require or request anything further from Applicants prior to examination, the Examiner is requested to contact Applicants' undersigned representative at the telephone number below. Otherwise, Applicants request early and favorable examination on the merits.

Jack P. Friedman  
Jack P. Friedman  
Reg. No. 44,688

Dated: 05/01/2022

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